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# Practical implementation of a digital signal processor controlled multilevel inverter with low total harmonic distortion for motor drive applications

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ABSTRACT

This paper presents a digital signal processor (DSP) based algorithm to generate three-level output voltage using H-Bridge multilevel inverter (MLI). The developed sinusoidal pulse width modulation (SPWM) scheme is employed to achieve lower harmonic contents in the output waveforms of inverter. Since SPWM scheme does not utilize vector positions, any pre-calculated switching states are not required. In addition to this advantage of conventional SPWM, modulators eliminate only base band harmonics due to regular control scheme. Therefore, neglecting the side band harmonics limits the efficiency of SPWM scheme. The harmonics located in the side bands of carrier frequency are also eliminated by the enhanced SPWM scheme proposed in this study. The validation of the modelled system is verified with the total harmonic distortion (THD) analyzes. The control algorithm is developed using TMS320F2812 DSP that is a 32-bit fixed-point processor operating at 150 MHz. The simulation and experimental results are compared to previous studies. The THD ratios of phase voltages and currents are measured loading the inverter with a three- phase 3 kW asynchronous motor. The lowest THD ratios of voltage and current are obtained at 1.9% and 0.4%, respectively.



## 1. Introduction

Since Nabae introduced them in 1981, multilevel inverters (MLI) constitute one of the most important research areas in power electronics. The first multilevel topology implemented is a neutral-point clamped inverter [1]. Up to now, several topologies such as symmetrical or asymmetrical have been developed besides control schemes. The major advantages of multilevel inverters are to achieve higher voltage levels to generate sine-like output voltages and high power outputs with lower $dv/dt$ stress on switches. Owing to minimizing common-mode voltages and electromagnetic interference (EMI), MLI topologies synthesize the output waveform with a better harmonic spectrum according to conventional inverter topologies [2–9]. Even though several MLI topologies are proposed in the literature, widely used topologies are classified in three main categories as neutral point clamped (NPC), flying capacitor (FC), and cascaded H-bridge (CHB). The diode clamped inverters, particularly the three-level structure, have a wide popularity in motor drive applications besides other multilevel inverter topologies. However, when the level exceeds the three, increased number of clamping diodes would be a limitation of complexity for the DC-MLIs. The FC-MLIs are based on balancing capacitors on the phase buses that are required at a number of $(m-1)\cdot(m-2)/2$ for an $m$-level inverter. In higher-level topologies, it will cause an increment on the number of required capacitor with DC-link voltage balancing issues. Among the three types of MLIs, the cascade inverter is the least component requiring topology for a given number of levels and consists of H-bridge cells to synthesize the desired voltage using several separate DC sources (SDCSs) obtained from batteries or fuel cells [10–15].

The most widely used modulation algorithms for multilevel inverters are selective harmonic elimination PWM (SHE-PWM), sinusoidal PWM (SPWM) and space vector PWM (SVM). SPWM scheme differs from others owing not to requiring complex mathematical preparations. While it is mandatory to calculate all switching vectors to define switching angles in SVM, SHE-PWM requires determining the switching angles for selected harmonics to be eliminated.

In SHE-based methods, the number of eliminated harmonics is determined with voltage levels and switching angles in each voltage level. Although multiple switching angles may be required in each cycle, most of the studies propose single switching angle due to complexity of mathematical equations. The sector number in a SVM algorithm is calculated using $3^n$ equation by assuming $n$ is the number of level. Thus, there are 27 sectors should be assigned for a 3-level SVM control while this number increases to 243 sectors in a

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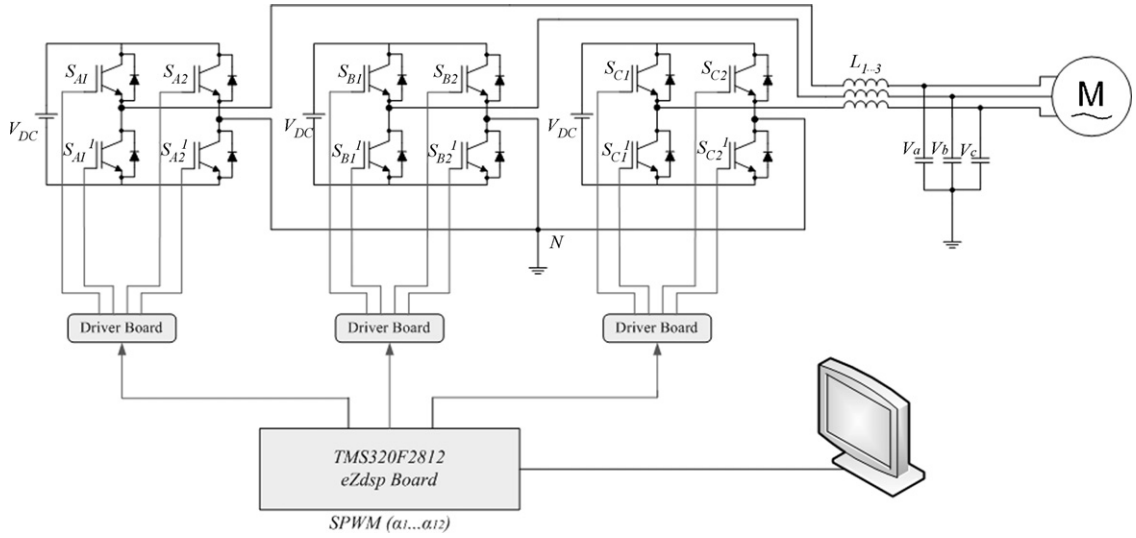


**Fig. 1.** Schematic diagram of the multilevel inverter system with DSP-based control.

5-level and to 2187 sectors in a 7-level MLI. This situation prevents to increase output level in an MLI topology that is controlled with SVM scheme.

The SPWM control scheme is based on comparing the phase shifted modulating signals with phase shifted or opposite triangular carriers to generate switching orders. Increasing the output level in any MLI topology can be performed using SPWM without complex mathematical operations [16–24]. Considering the topologies and control schemes examined above, the most proper combination selected is SPWM controlled H-bridge topology owing to harmonic elimination features of SPWM scheme and easily implementable structure for higher-level outputs of H-bridge topology. In spite of these advantages, regular SPWM does not consider side band harmonics that are caused by carrier frequency and overlapped with output waveforms while generating the switching orders. In this study, an enhanced SPWM modulation scheme is proposed in order to eliminate side band harmonics those increase the current and voltage THD ratios. In addition to eliminating side band harmonics of carrier frequency, even side band harmonics that are generated by multiples of carrier frequency are also eliminated with the developed analytical model of SPWM scheme.

The three-level H-bridge MLI implemented in this study is commutated with enhanced SPWM algorithm that is processed by TMS320F2812 DSP. The microprocessor used is capable to provide 12 channels PWM outputs. The switching frequency ($f_{sw}$) is adjusted to various values up to 10 kHz while modulation index ($m_i$) is fixed in the linear modulation area. The load structure of the MLI is determined with a 3 kW asynchronous motor. The harmonic and power analyses are performed using Fluke 43B Power Quality Analyser and Rigol DS1100 Series Oscilloscope. The obtained experimental results are compared to similar studies in order to validate the performance of the implemented system in terms of harmonic ratios and power issues.

## 2. The system implemented with DSP-control

The system designed is primarily modelled using Matlab-Simulink to constitute the modulation algorithm. The main parts of the inverter implemented are MLI circuit, driving boards and DSP-based control section. Since it requires less switching devices and can be easily developed, the main power circuit is assembled utilizing the cascaded H-bridge MLI topology in the study. Each phase legs are constructed using an H-bridge cell to generate 3-level staircase waveform at the phase outputs.

Unlike NPC and FC topologies, the H-bridge topology requires separate DC source (SDCS) to supply each cell. The SDCSs of implemented system are constituted using isolation transformers with 2 kVA rated power for each. The implemented single-phase uncontrolled full-bridge rectifiers generate DC voltages using the three-phase AC line voltage achieved over a variac.

### 2.1. MLI circuit and driving board

The H-bridge cells are formed with 2MBI150U2A-060 insulated gate bipolar transistors (IGBT) of Fuji Electric. The collector–emiter voltage of IGBT modules is 600 V while collector current is 150 A in continuous conduction mode. The gate-emitter voltage is ±20 V, turn-on and turn-off times are about 0.40 μs [25].

The gate driver circuit is developed using EXB-840 integrated circuit that is capable to drive IGBTs up to 1200 V with isolated gate supplies [26]. The phase outputs of inverter are filtered with 1 mH-6 μF passive LC filter as shown in Fig. 1. The output voltage waveform is controlled by phase shifting process of the each half bridge in H-bridges of Fig. 1. The phase shifting process of the enhanced SPWM provides to generate three-phase output voltage levels in a square waveform that are $2\pi/3\,\mathrm{rad\,s^{-1}}$ phase shifted. In case of the reference modulating signals are arranged with the proper phase shifting ratios, the phase voltages and currents are defined with equations as given in Eqs. (1)–(6) [3,20],

$$V_{a0} = m_i.\frac{V_{dc}}{2}\cos(\omega_0 t) \tag{1}$$

$$V_{b0} = m_i.\frac{V_{dc}}{2}\cos\left(\omega_0 t - \frac{2\cdot\pi}{3}\right) \tag{2}$$

$$V_{c0} = m_i.\frac{V_{dc}}{2}\cos\left(\omega_0 t - \frac{4\cdot\pi}{3}\right) \tag{3}$$

$$i_a(t) = \hat{I}\cos(\omega_0 t - \theta) \tag{4}$$

$$i_b(t) = \hat{I}\cos(\omega_0 t - \frac{2.\pi}{3} - \theta) \tag{5}$$

$$i_c(t) = \hat{I}\cos\left(\omega_0 t - \frac{4\cdot\pi}{3} - \theta\right) \tag{6}$$

where $m_i$ defines the modulation index, $V_{dc}$ is the DC supply voltage, $\hat{I}$ is the peak value of phase current, and $\theta$ is the phase shift between current and phase voltage.

### 2.2. DSP-based control

eZdsp F2812 board generates the SPWM switching signals that are applied to IGBT gate drive circuit. The PWM generation in a DSP is controlled by General Purpose (GP) timers, which perform the operations under the control of Event Manager-A (EVA) with GP Timer 1/2 and Event Manager-B (EVB) with GP Timer 3/4. All the GP Timers are 16-bit which are named as TxCNT for up-down counter, TxCMPR for timer-compare operation, TxPR for timer-period register, and TxCON register for timer-control register.

The other units of Event Managers are full-compare/PWM units, capture units, and quadrature-encoder pulse (QEP) circuits. Each Event Manager of F2812 DSP is capable to generate up to six PWM outputs separately, thus the Deadband Generation can be individually enabled or disabled for each compare unit outputs. The deadband-generator circuit generates two outputs (with or without deadband zone) for each compare unit output signals [27–33].

## 3. SPWM modulation scheme and DSP algorithm

The SPWM scheme is one of the most popular modulation techniques among the others applied in power switching inverters. The fundamental frequency SPWM control method is proposed to minimize the switching losses. In SPWM scheme, a sinusoidal reference waveform is compared with a triangular carrier waveform to generate switching sequences. Each switching angles ($S_{sw}(t)$) are calculated by Fourier series as seen in Eq. (7) in order to eliminate harmonic contents in the base-bands,

$$S_{sw}(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty}(a_n \cos(n\omega t) + b_n \sin(n\omega t)) \tag{7}$$

where $a_0$ is the average DC value of the switching signal. The Fourier coefficients $a_0$, $a_n$, and $b_n$ are given by Eqs. (8)–(10):

$$a_0 = \frac{1}{\pi}\int_{-\pi}^{\pi} S_{sw}(t)\ dt \tag{8}$$

$$a_n = \frac{1}{\pi}\int_{-\pi}^{\pi} S_{sw}(t)\cos(n\omega t)\ dt \tag{9}$$

$$b_n = \frac{1}{\pi}\int_{-\pi}^{\pi} S_{sw}(t)\sin(n\omega t)\ dt \tag{10}$$

The coefficient $c_n$ of the $n$th harmonic component of the signal $S_{sw}(t)$ is defined as depicted in Eq. (11);

$$c_n = a_n + jb_n \tag{11}$$

Although base band harmonics are eliminated, the modulation bandwidth of periodic signal and the side band harmonics are neglected in conventional SPWM. However, bandwidth of a modulated signal is theoretically infinite [34,35] that causes harmonics in a modulated signal. Elimination of these harmonics can be done with filtering the carrier and modulating signals during modulation process. The digital modulation filtering methods are Chebyshev, Butterworth, Bessel, Elliptic, and ITEA filter, which use the minimum integral of time. The conventional SPWM method is enhanced using Bessel filtering function to eliminate side band harmonics in this paper. Bessel function yields solution to Helmotz and Laplace equations. The switching states are obtained with interpolation of samples that are used to regenerate the sampled modulation signals in the developed mathematical model of SPWM. Such an interpolation in discrete time domain is equivalent to filtering process in frequency domain. The harmonic elimination feature of the enhanced modulation scheme is increased by adding digital filtering operations with interpolation method. Bessel functions are defined in series expansion form in electromagnetic, telecommunication, and power systems. 1st order Bessel function is defined by Gradshteyn and Ryzhik as seen in Eq. (12) [36–39].

$$J_\alpha(x) = \left(\frac{x}{2}\right)^\alpha \sum_{k=0}^{\infty}\frac{(-1)^k}{k!\,\Gamma(\alpha+k+1)}\left(\frac{x}{2}\right)^{2k} \tag{12}$$

where $\Gamma$ is the gamma function and $\alpha$ is the degree of Bessel function. Bessel function is rearranged for $\alpha = 0$ and $\alpha = 1$ orders as expressed in Eqs. (13) and (14);

$$J_0(x) = \sum_{k=0}^{\infty}(-1)^k\frac{x^{2k}}{2^{2k}k!(k+1)!} \tag{13}$$

$$J_1(x) = \frac{x}{2}\sum_{k=0}^{\infty}\frac{(-1)^k x^{2k}}{2^{2k}k!(k+1)!} \tag{14}$$

The equivalent integrative definition of first kind and $\alpha$ ordered Bessel function is obtained as seen in Eq. (15) [40–42],

$$J_\alpha(x) = \left(\frac{x}{2}\right)^\alpha \frac{1}{\sqrt{\pi}\,\Gamma\left(\alpha+(1/2)\right)}\int_{-1}^{1}(1-\omega^2)^{\alpha-(1/2)}\cos(\omega x)\,d\omega \tag{15}$$

Firstly, Eq. (15) that is obtained using the general form of Bessel function is added to analytical model of regular SPWM equation to eliminate the odd ordered harmonic contents as given in Eq. (16).

$$V_0(t) = \left[\frac{m_i V_{dc}}{2}\cos(\omega_r t)\right] + \left[\frac{2V_{dc}}{\pi}\sum_{k=1}^{\infty}J_0\left(k\cdot m_i\frac{\pi}{2}\right)\sin\left(k\cdot\frac{\pi}{2}\right)\cos(k\cdot\omega_c t)\right] \tag{16}$$

where, $m_i$ = modulation index, $V_{dc}$ = DC supply voltage, $\omega_r$ = reference frequency, $\omega_c$ = carrier frequency, $J_0$ = Bessel function

First part of Eq. (16) is the fundamental component that is also known as conventional SPWM model. Second part of the equation defines amplitude of harmonics that are located at the base and multiples of carrier frequency. The Bessel function arranged in this way eliminates the harmonics caused by fundamental and side bands of carrier in SPWM modulation. According to modulation theory, a square wave in time domain generates side bands over its own bandwidths in frequency domain that is explained with sinc function [35]. Therefore, side band harmonics of carrier frequency are also required to be eliminated in addition to carrier harmonics analysed in Eq. (16). The enhanced SPWM modulation scheme is obtained as shown in Eq. (17) by considering the additional Bessel function that provide to eliminate side band harmonics of carrier additionally to Eq. (16). The output periodic voltage waveform, $V_0(t)$, consists of three major terms to eliminate possible harmonic contents in generated AC output. The first term of Eq. (17) gives the amplitude of fundamental component while the second part is depicting the amplitude of the harmonics at the carrier frequency and the multiples of carrier. The last term indicates the amplitudes of the harmonics in the sidebands around each multiples of the carrier frequency. The modulation algorithm is developed using Eq. (17) in order to eliminate side-band harmonics. The additional important point to be considered in the modulator design is amplitude distortion. The amplitude distortion is caused by the input DC voltage source variation and has the most significant impact on the "on–off" spectral errors. For the voltage source inverter (VSI), the amplitude distortion of the developed SPWM waveforms will decline the amplitude of the fundamental component and eliminates the unexpected low order harmonic contents.

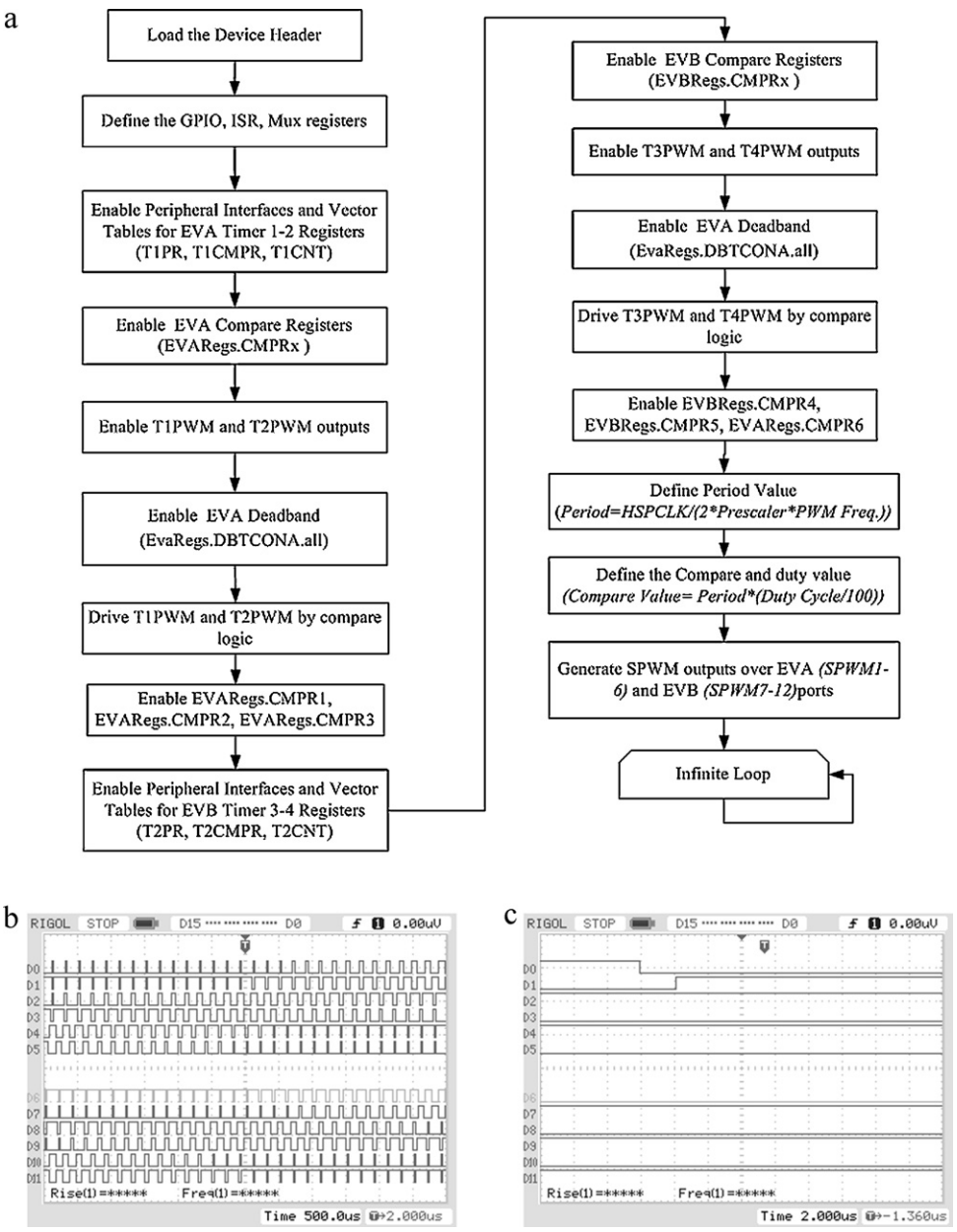


**Fig. 2.** SPWM generating with eZdsp F2812; (a) Flowchart of SPWM algorithm executed in DSP. SPWM generating with eZdsp F2812, (b) 12-channel SPWM outputs of DSP with 5 kHz switching frequency and 0.8 modulation index, (c) 2 μs dead-band generated controlling the registers of DSP.

$$V_0(t) = \frac{m_i V_{dc}}{2}\cos(\omega_r t) + \frac{2V_{dc}}{\pi}\sum_{k=1}^{\infty} J_0\left(k\cdot m_i\frac{\pi}{2}\right)\sin\left(k\cdot\frac{\pi}{2}\right)\cos(k\cdot\omega_c t)$$
$$+\frac{2V_{dc}}{\pi}\sum_{k=1}^{\infty}\sum_{l=\pm1}^{\pm\infty}\frac{Jn\left(k\cdot m_i(\pi/2)\right)}{k}\sin\left[\left((k+l)\cdot\frac{\pi}{2}\right)\right]\cos(k\cdot\omega_c t + l\cdot\omega_r t)\Bigg\} \quad (17)$$

where, $m_i$ = modulation index, $V_{dc}$ = dc supply voltage, $\omega_r$ = sinusoidal reference frequency, $\omega_c$ = triangular reference frequency, $J_0$, $J_n$ = Bessel function.

The term of modulation index ($m_i$) given in Eq. (18) is the ratio of the peak values of the modulating signal, $V_m$, to triangular carrier signal, $V_c$.

$$m_i = \frac{V_m}{V_c} \quad (18)$$

The frequency of modulating signal defines the desired line voltage frequency at the inverter output. The line-to-line voltage rates of inverter are determined according to modulation indexes ($m_i$) those define the operating areas in linear modulation ($m_i \leq 1$) or over-modulation ($m_i > 1$) ranges. The line-to-line voltages are limited to ($\sqrt{3}V_d/2$) of DC line in linear modulation range and limits to ($4/\pi$). ($\sqrt{3}V_d/2$) in over modulation range [5,20]. In the linear modulation range, the SPWM modulator acts as an amplifier with the gain parameter ($G$) that is defined in Eq. (19),

$$G = \frac{0.5 m_i V_d}{V_p} = \frac{0.5 V_d}{V_t} \quad (19)$$

The gain yields 78.55% of the peak value of the square voltage while $m_i = 1$. In SPWM control technique, the output voltage

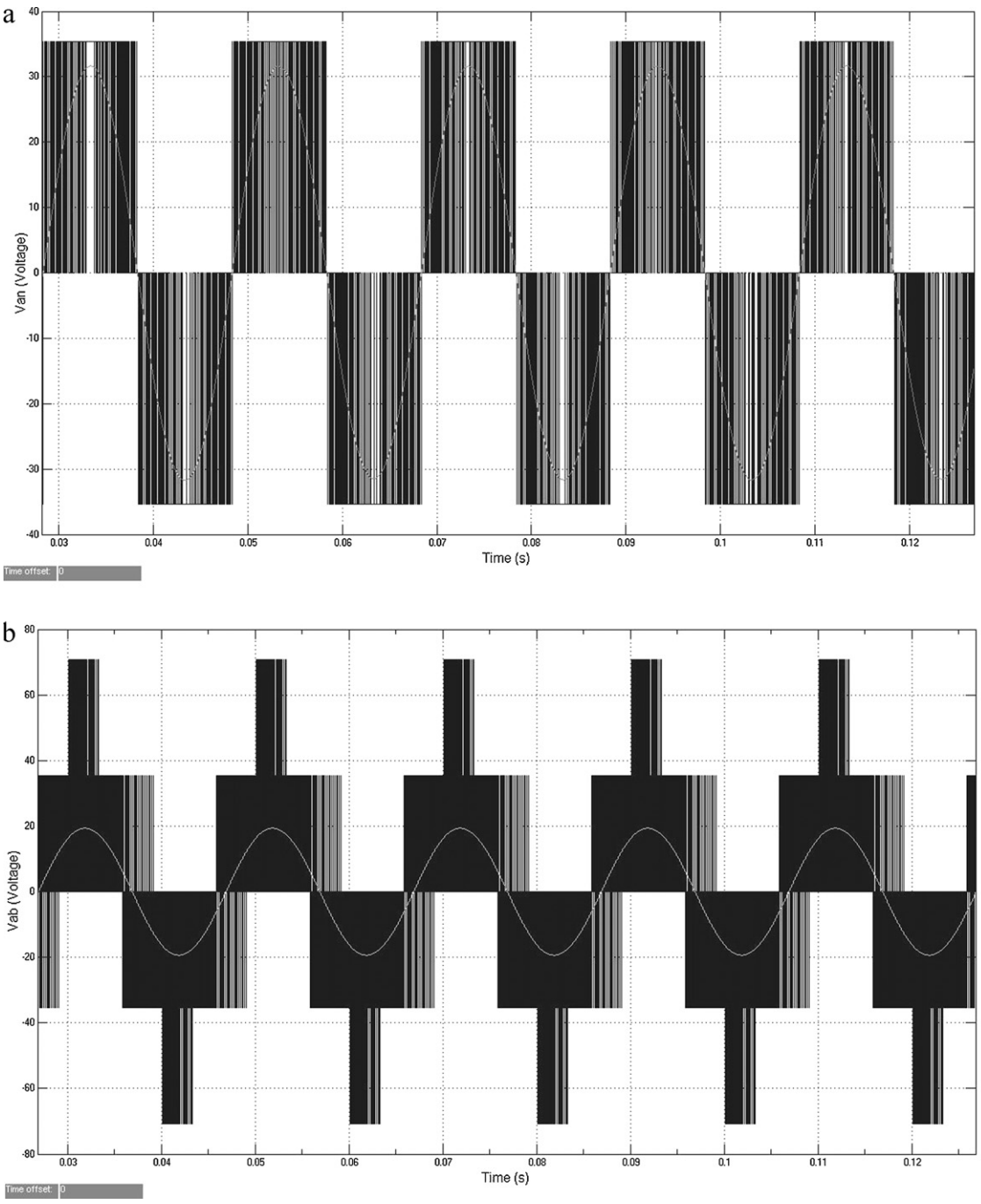


**Fig. 3.** The waveforms of MLI simulation; (a) phase voltage of inverter, (b) line-to-line and rms voltages of inverter.

is defined as given in Eqs. (20) and (21) in linear modulation range and the over-modulation, respectively [7,14,18,19,43,44].

$$V_{AB} = V_{BC} = V_{CA} = m_i \frac{\sqrt{3}V_d}{2} \quad 0 < m_i \leq 1 \tag{20}$$

$$\frac{\sqrt{3}V_d}{2} < V_{AB} = V_{BC} = V_{CA} < \frac{4}{\pi}\frac{\sqrt{3}V_d}{2} \quad m_i \geq 1 \tag{21}$$

The flowchart of DSP program is shown in Fig. 2(a). The EVA and EVB Event Manager Modules of DSP are main controllers of the evaluated algorithm. The Timer 1 and Timer 2 of EVA generate the first six SPWM switching sequences, while Timer 3 and Timer 4 of EVB generate the last six SPWM signals. The period registers of each timer provide to set the switching frequency. The values of period and compare registers required to be calculated to create PWM signals with a specific frequency and duty cycle. In order to calculate the values, the proper SYSCLKOUT frequency is needed to be known which is at 150 MHz for TMS320F2812 DSP. The calculation of period value and compare values are given in Eqs. (22) and (23) [30–33];

$$\textit{Period value} \quad (P.V.) = \frac{HSPCLK}{2 * (PWM\ Freq.)} \tag{22}$$

where, HSPCLK = SYSCLKOUT/(Input Clock Prescaler).

$$\textit{Compare value} = (P.V.)^{*}(\textit{Duty Cycle}/100) \tag{23}$$

When the algorithm is executed on DSP, the output signals of EVA and EVB module are obtained as seen in Fig. 2(b).

The upper part of scope screen shows the first six SPWM switching signals generated by EVA module and the lower part shows the left signals generated by EVB module. Fig. 2(c) depicts the 2 μs deadband added to switching sequences in order to prevent spectral losses. The deadband value can be re-arranged adjusting the values of programmable deadband generator as given below for 2 μs delay [45,46];

```
EvaRegs.DBTCONA.bit.DBTPS = 0x0005;
EvaRegs.DBTCONA.bit.DBT = 0x0005;
EvbRegs.DBTCONB.bit.DBTPS = 0x0005;
EvbRegs.DBTCONB.bit.DBT = 0x0005;
```

## 4. Simulation studies

The analytical design of MLI is verified using Matlab/Simulink. The mathematical model of SPWM modulator is developed considering a switching bandwidth between 0 and 040 kHz to commutate H-bridges. The switching frequency of SPWM modulator is limited between 1 kHz and 10 kHz, and modulation indexes are selected in $0.6 \leq m_i \leq 1.2$ ranges to analyze the effect of $f_{sw}$ and $m_i$ on THD of inverter. The power block of MLI is constituted using three separate H-bridges and 12 switching orders are applied. The modulator block consist two sections that are modulating signal generator with the proper phase shifting and the second section of carrier generator and comparator to compare the modulating and carrier signals. The generated switching signals are applied to power block over

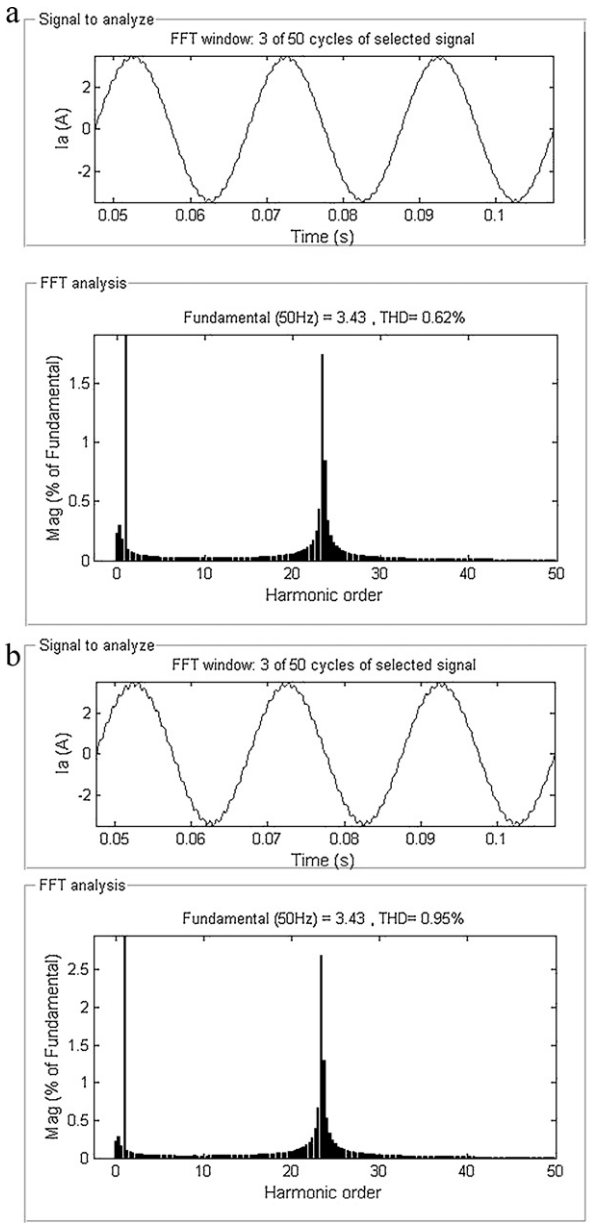


**Fig. 4.** The $THD_i$ analyses while $m_i = 0.8$; (a) $f_{sw} = 5$ kHz, (b) $f_{sw} = 10$ kHz.

**Table 1**
Motor parameters.

| Parameter | Value (SI) |
|---|---|
| Rated power | 3 kW |
| Rated speed | 1430 rpm |
| Stator resistance | 1.405 Ω |
| Rotor resistance | 1.395 Ω |
| Stator inductance | 0.0058H |
| Rotor inductance | 0.0058H |
| Mutual inductance | 0.1722H |
| Poles | 4 |

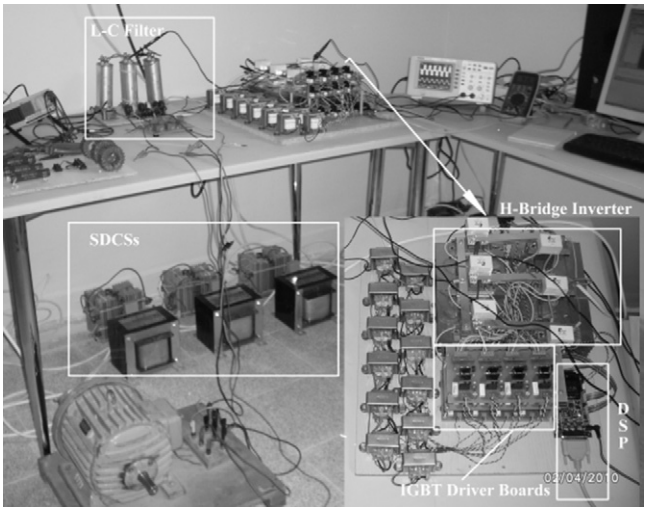


**Fig. 5.** Experimental set-up.

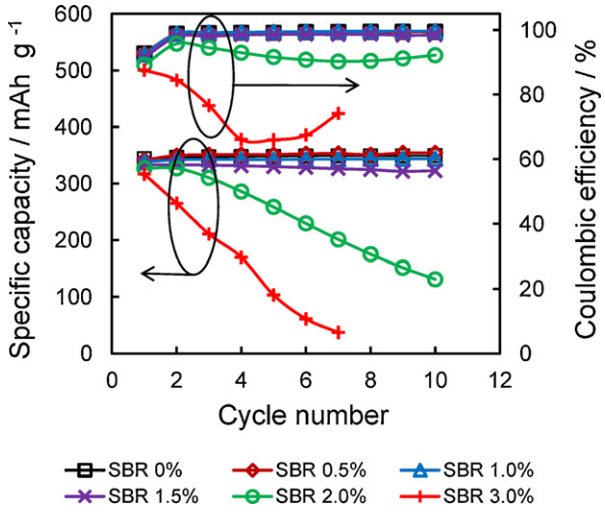


**Fig. 6.** The cycle performance of SNG12 anode with PAALi binder doped by different amounts of SBR.

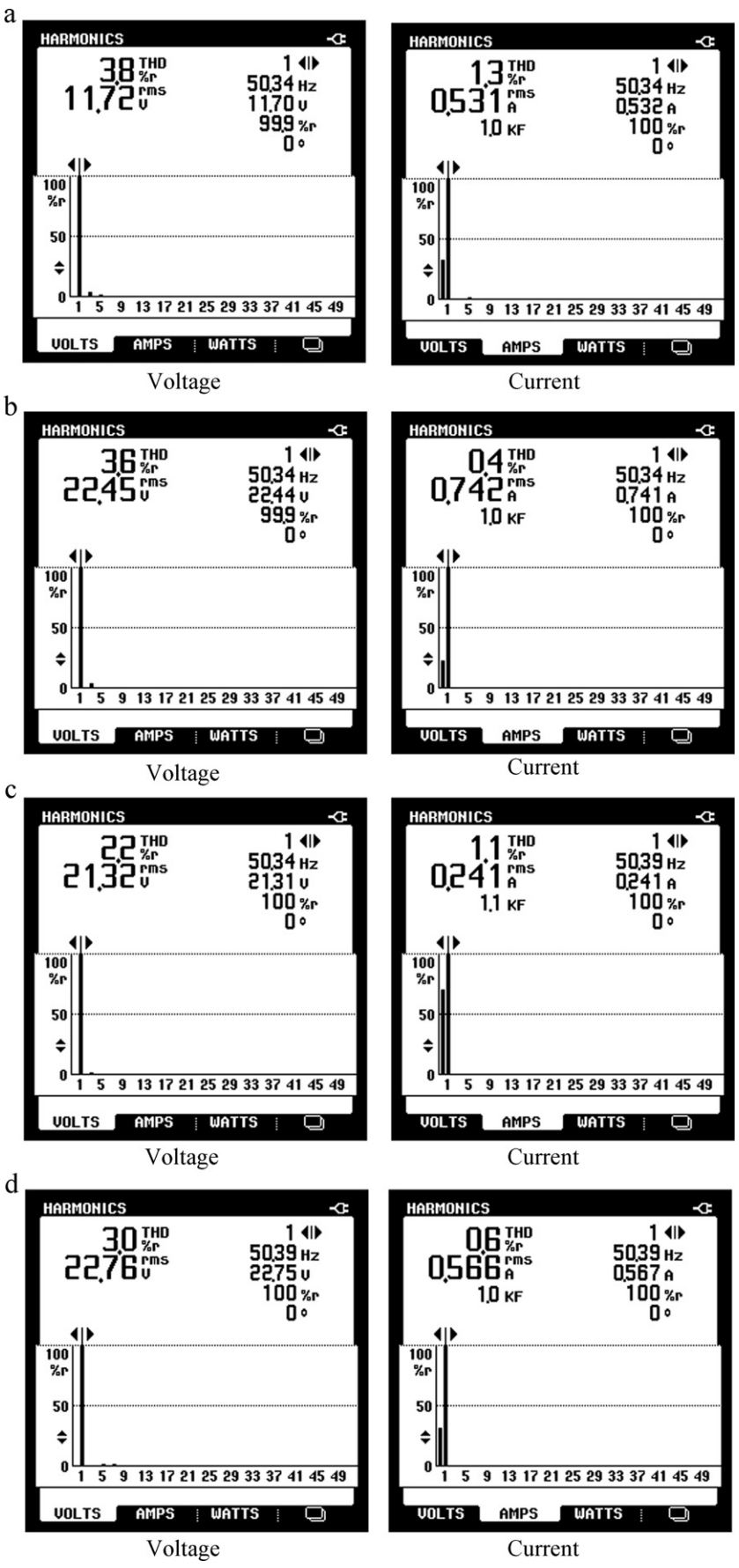


**Fig. 7.** Voltage and current THD analyses of MLI under $f_{sw}$ = 5 kHz and $m_i$ = 1 condition; conventional SPWM, (b) developed SPWM.

4-channels for each phase of MLI. The measured phase voltage, line-to-line voltage and current THD analyses waveforms are shown in Fig. 3. The supply voltage of SDCSs primarily set to 50 V in the simulation. The phase voltage shown in Fig. 3(a) is measured about 71 $V_{p-p}$, while the line-to-line voltage is about 145 $V_{p-p}$ generating 5-level output waveform as depicted in Fig. 3(b). The parameters of 3-phase asynchronous motor used in the simulation are shown in Table 1.

The line current THD ($THD_i$) analyses are carried out operating the motor at full load. Fig. 4(a) illustrates the $THD_i$ analyses performed by controlling the inverter at 5 kHz $f_{sw}$ with 0.8 $m_i$ value. The measured $THD_i$ value is 0.62% at these operating conditions. When $f_{sw}$ increased to 10 kHz, the $THD_i$ value increases to 0.96% since the modulator could not eliminate side band harmonics properly as seen in Fig. 4(b). The output current and voltage values are increased in over-modulation range since $m_i$ is over 1, but the THD rates are changed nonlinearly.

## 5. Experimental studies

The experimental set-up is illustrated in Fig. 5. Each SDCS required per phase of MLI is constructed using isolation transformers those provide 2 kVA rated power and supplied by a three-phase variac. The transformer outputs are rectified with single-phase rectifiers that are assembled with 71HFR60 diodes of International Rectifier. The lower right-hand side of Fig. 5 displays the top view of MLI board containing IGBT driver board, H-bridge connections and TMS320F2812 DSP board. The phase voltages are filtered using an L-C filter bank, which is constituted with 1 mH inductor and 6 μF capacitor. The asynchronous machine used to load the inverter is a 3 kW three-phase AEG with the parameters given in Table 1. The experimental studies are limited to 10 kHz at full load operations. The modulation index is respectively set to 0.6, 0.8, and 1 at 5 kHz switching conditions.

The phase voltages, phase currents and harmonic analyses are shown in Figs. 6 and 7. The SDCSs are adjusted to 80 V in experimental studies to generate AC phase voltages seen in Fig. 6(a). The peak-to-peak value of phase voltage is measured at 110 V while the rms value of filtered phase voltage is about 40 V. The line voltage measured between R–S phases is shown in Fig. 6(b). The peak-to-peak value of 5-level line voltage and rms values are measured as 198 V and 53.3 V, respectively. The phase-shifting between filtered R–S phases and Fast Fourier Transform (FFT) curves are depicted in Fig. 6(c). The FFT spectrum displays the amplitude of third harmonic around 0.4 V while other side band harmonics are eliminated.

The developed SPWM algorithm is compared to conventional SPWM in terms of harmonic elimination by applying with same $f_{sw}$ and $m_i$ values to MLI. Fig. 7(a) shows the voltage and current THD spectrums of conventional SPWM controlled MLI while THD analyses of MLI that is switched using developed SPWM are represented in Fig. 7(b). It is seen in voltage spectrum of Fig. 7(a) that almost all the side band harmonics up to 40th order affect phase voltage. The current THD analysis of MLI with conventional SPWM control exhibits similar situation with increased third and fifth harmonic orders. Both of the FFT analyses given in Fig. 7(a) shows that conventional SPWM is not able to eliminate higher order harmonics that are caused by amplitude distortion. In addition to this, effective side band harmonics are also seen in FFT spectrum that increases THD ratio of waveforms. The experimental studies are performed again with the developed SPWM algorithm to determine the success of enhanced algorithm. The analysis results shown in Fig. 7(b) represents voltage and current THD spectrums respectively. The developed SPWM algorithm properly eliminates side band harmonics that are seen in conventional SPWM experiments. The performed experimental analyses show that developed SPWM algorithm decreases phase voltage THD from 16.5% to 2.2%, and phase current THD from 19.2% to 1.1% according to conventional SPWM.

The THD analyses under various operating conditions are illustrated in Fig. 7(a)–(d). Even though the typical switching frequency is set to 5 kHz, additional analyses are shown in Fig. 7(d) for 10 kHz switching frequency with 0.8 $m_i$. The phase voltage THD ($THD_v$) and phase current THD ($THD_i$) ratios are measured 3.8% and 1.3%, respectively, while the $f_{sw}$ = 5 kHz and $m_i$ = 0.6 in Fig. 7(a). In this situation, third and fifth harmonics are seen in phase voltage and only fifth harmonic exists with a quite low value in current FFT spectrum. The $THD_v$ value is decreased to 3.6% and $THD_i$ ratio is measured as 0.4% when the $m_i$ increased to 0.8 (Fig. 7(b)). The increment of $m_i$ from 0.6 to 0.8 eliminates 5th harmonics in voltage and current spectrums by comparing to Fig. 7(a). The over-modulation harmonics seen in Fig. 7(c) are 2.2% for $THD_v$ and 1.1% for $THD_i$. The analyses carried out with 5 kHz switching frequency prove the minimum $THD_i$ value when the $m_i$ is set to 0.8. Another analyses which are performed by setting $m_i$ to 0.8 and increasing the $f_{sw}$ to 10 kHz increased $THD_i$ to 0.6% as depicted in Fig. 7(d). Increased $f_{sw}$ prevents to eliminate side band harmonics according to 5 kHz where seventh harmonic exist in addition to fifth one in phase voltage. All the measurements are obtained while the motor was rotating at 1435 rpm. The simulation and experimental results provide proper THD ratios to the limits of IEEE-519 and IEC 61000-3-2 (formerly IEC 555-2) [47,48].

The measured results are compared to relevant previous studies in order to verify the performance of the implementation. The proposed modulation algorithm executed on TMS320F2812 DSP processor supplies lower THD ratios without requiring any prepared or pre-calculated switching angles according to the previous studies such as [8–10,31].

In addition to this, the SPWM scheme supplies a robust control feature in the mean of eliminating the side-band harmonics even up to 10 kHz switching frequency.

The proposed system also managed out to eliminate almost all harmonic contents only with a 3-level topology while similar studies reach this value with 7 or higher level inverters [12,13].

## 6. Conclusion

In this paper, an enhanced SPWM algorithm executed on a TMS320F2812 is proposed with H-bridge MLI application. The implemented algorithm successfully eliminates the base band and side band THDs by calculating the switching angles in each period. The SPWM control scheme is also compared to relevant studies implemented with SHE-PWM and SVM. The enhanced SPWM algorithm removes any pre-calculation requirements according to mentioned control schemes besides expanding the switching band up to 10 kHz. The switching sequences are determined with online calculation instead of using a look-up table that is widely used in the previous applications.

The experimental verification of the algorithm modelled using Simulink is performed using a 3 kW asynchronous motor load. The minimum $THD_i$ ratio is measured as 0.4% while the switching frequency ($f_{sw}$) is 5 kHz and modulation index ($m_i$) is 0.8. The $THD_i$ ratio is obtained as 0.6% when the $f_{sw}$ is increased to 10 kHz. The harmonic contents seen in $THD_v$ measurements are third and fifth orders for 0.6 modulation index. The fifth harmonics are eliminated when the $m_i$ value is set to 0.8 and 1 at 5 kHz switching frequency. The additional $THD_v$ harmonic contents at 10 kHz switching frequency are determined as fifth and seventh ones. Even though all the measurements prove international standard such as IEEE-519 and IEC 61000-3-2, the most proper operating condition can

be defined as 5 kHz for switching frequency with 0.8 modulation index.

It is possible to implement the proposed SPWM algorithm in order to design five and 7-level inverters using asymmetrical topologies without changing the processor for future works.

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